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Description

RAISED STI PROCESS FOR MULTIPLE GATE OX AND SIDEWALL PROTECTION ON STRAINED Si/SGOI STRUCTURE WITH ELEVATED SOURCE/DRAIN

BACKGROUND OF INVENTION

[0001] The present invention relates to semiconductor devices, and more particularly to a strained Si/silicon germanium-on-insulator (SGOI) structure having an elevated source/drain region and a raised trench isolation region. The present invention also relates to a method of fabricating such a strained Si/SGOI structure.

[0002] Improvements in transport properties, i.e., carrier mobility, through strain have been demonstrated in the operating characteristics of field effect transistors (FETs). For complementary metal oxide semiconductor (CMOS) devices, an improvement in device characteristics through carrier mobility has significant potential for the fabrication

of very high-speed devices. Strained silicon on a relaxed SiGe substrate is one system where such an improvement occurs.

[0003] Experimental research on enhanced carrier mobility MOSFETs caused by strain has concentrated on a strained Si layer grown on a relaxed SiGe layer that is located on a bulk semiconductor wafer. MOSFETs fabricated using a strained Si/SiGe system exhibit the following disadvantages: (1) High source/drain junction leakage--the FET source/drain junctions, as well as the channel region, are formed in a strained Si area resulting in higher junction leakage. (2) The Si/SiGe system MOSFET process is not compatible with mainstream CMOS fabrication techniques requiring specially prepared substrates using molecular beam epitaxy. (3) The Si/SiGe system MOSFET process is costly with low production rate.

[0004] In addition to the above mentioned drawbacks with strained Si/relaxed SiGe/bulk wafer structures, prior art structures including strained Si formed on a SiGe-on-insulator (SGOI) template (also referred to herein as a strained Si/SGOI structure) exhibit the following unique problems:

[0005] (A) Loss of trench isolation oxide during a multiple gate

oxide thickness process (which requires an oxide wet etch selectively with the resist mask, adding trench isolation height). A wider range of trench isolation height requires more etching of the polySi gate resulting in potential gate oxide punchthrough.

[0006] (B) A trench isolation divot forms at the strained Si/trench isolation interface. This can create a short circuit between the strained Si islands due to a gate polySi stringer.

[0007] (C) A chemical mechanical polishing (CMP) uniformity restriction is imposed or a narrow process window is obtained.

[0008] (D) A narrow polySi gate over etching window.

[0009] (E) A limitation of thermal budget during pad oxide growth.

[0010] (F) Strained Si sidewall exposure and Si loss.

[0011] In view of the drawbacks mentioned with the prior art, there is a need for providing a new and improved method of fabricating a strained Si/SGOI structure that overcomes the aforementioned issues recited under items (A)-(F).

SUMMARY OF INVENTION

[0012] The present invention resolves the problems with the prior art method mentioned above by reversing the pro-

cess sequence of gate dielectric and trench isolation formation. In a conventional process, the gate dielectric, i.e., oxide, is formed after formation of the trench isolation region, restricting the amount of trench dielectric oxide removal during the multiple gate oxide processing. In the prior art process, an oxide divot is typically formed in the strained Si/SGOI structure, which can result in a short circuit with a neighboring active area when a polySi stringer is present in the divot.

[0013] In the present invention, the gate formation process can be done without any restriction of oxide removal. Hence, items (A), (B) and (E) mentioned above are resolved. Moreover, the gate polySi top surface is planarized in the present invention by a two step gate poly deposition (before and after trench isolation) thereby eliminating unnecessary poly over etching. Also, the inventive structure allows for a higher trench isolation height as compared to the conventional process. Hence, the present invention resolves the issues mentioned under items (C)-(D) above. Furthermore, due to the higher trench isolation height that can be achieved in the present invention, a disposable nitride spacer can be employed which protects the sidewalls of the strained Si thereby resulting in little or no

Si loss at the isolation trench edge.

[0014] In broad terms, the present invention provides a method of fabricating a strained Si/SGOI structure that comprises the steps of:

[0015] providing a structure including a silicon germanium-on-insulator (SGOI) substrate, a strained Si layer atop the SGOI substrate, a gate dielectric atop the strained Si layer, a gate polySi atop the gate dielectric and a pad nitride atop the gate dielectric;

[0016] forming a first stack of said pad nitride, said gate polySi, said gate dielectric, said strained Si, and a relaxed SiGe layer of the SGOI substrate;

[0017] forming a trench oxide in regions adjacent to said first stack;

[0018] removing said pad nitride from said first stack to expose said gate polySi layer;

[0019] forming a material layer comprising a polySi layer, an insulator, such as an oxide, and a cap nitride on said exposed gate polySi layer and said trench oxide, said polySi layer is in contact with said gate polySi layer;

[0020] forming a second stack comprising said cap nitride, said insulator, said polySi layer, and said gate polySi layer, said second stack is located atop said gate dielectric; and

[0021] forming a raised source/drain region on said strained Si layer in regions adjacent to said second stack, wherein during said forming exposed sidewalls of the trench oxide are protected with a sacrificial nitride spacer.

[0022] In some embodiments, and during the forming of the first stack, the relaxed SiGe layer can be etched so that a recess region is formed beneath the strained Si layer.

[0023] Following the formation of the raised source/drain region, the sacrificial nitride spacers are removed forming voids in the structure that can be subsequently filled with a nitride fill material. Oxide spacers are then formed about the second stack.

[0024] In addition to the above method, the present invention also relates to the strained Si/SGOI structure that is formed by performing the aforementioned processing steps. In broad terms, the inventive strained Si/SGOI structure comprises:

[0025] an active device region comprising a relaxed SiGe layer, a strained Si layer located atop the relaxed SiGe layer, a raised source/drain region located atop a portion of said strained Si layer, and a stack comprising at least a gate dielectric and a gate polySi located on another portion of the strained Si layer; and

[0026] a raised trench oxide region surrounding said active device region.

Brief Description of Drawings

[0027] FIGS. 1A-1K are pictorial representations (through cross sectional views) illustrating the basic processing steps employed in one embodiment of the present invention.

Detailed Description

[0028] The present invention, which provides a strained Si/SGOI structure having an elevated source/drain region and a raised trench isolation region and a method of fabricating the same, will now be described in greater detail by referring to drawings that accompany the present application.

[0029] Reference is first made to FIG. 1A, which illustrates an initial structure 10 that is employed in the present invention. The initial structure 10 comprises a SiGe-on-insulator (SGOI) substrate 12, a strained Si layer 20 located on a surface of the SGOI substrate 12, and a gate dielectric 22 located on a surface of the strained Si layer 20. As shown, the SGOI substrate 12 includes a Si-containing substrate layer 14, an insulating layer 16, and a SiGe layer 18 that is in a relaxed state.

[0030] The SGOI substrate 12 can be fabricated using any con-

ventional process in which a relaxed SiGe layer is formed atop a surface of an insulating layer. In one embodiment, for example, the SGOI substrate 12 can be formed by thermally growing a SiGe layer, which is relatively thick, on a silicon-on-insulator (SOI) layer of a SOI substrate and then relaxing the SiGe layer by annealing/oxidation.

[0031] In another embodiment, for example, the SGOI substrate 12 can be formed by wafer bonding and/or by oxygen ion implantation.

[0032] Co-assigned U.S. Application Serial No. 10/662,028, filed September 12, 2003, the entire content of which is incorporated herein by reference, discloses yet another possible way in which the SGOI substrate 12 can be fabricated. In accordance with U.S. Serial No. 10/662,028, a structure comprising a Si-containing substrate having a hole-rich region and a Ge layer located thereon is first provided. Next, the hole rich region is converted into a porous region utilizing an anodization process and then the structure is annealed such that the porous region is converted into a buried oxide region, while simultaneously forming a relaxed SiGe alloy layer atop the buried oxide.

[0033] In yet another method, a thermal mixing process such as described, for example, in co-assigned U.S. Application

Serial No. 10/448,947, filed May 30, 2003, co-assigned U.S Application Serial No 10/055,138, and co-assigned U.S Application Serial No. 10/669,601, filed October 29, 2003 can be used in forming the SGOI substrate; the entire content of each of the aforementioned U.S. Applications is incorporated herein by reference. In the thermal mixing process, ions such as oxygen are first implanted into a Si-containing substrate to form an implanted ion rich region. Next a Ge-containing layer such as a SiGe alloy or pure Ge, is formed atop the implanted structure, and then the structure is annealed under conditions that permit the formation of a Ge diffusion barrier in the Si-containing substrate, while simultaneously causing interdiffusion (and hence intermixing) of Si and Ge forming a relaxed SiGe layer atop the Ge diffusion barrier.

[0034] Notwithstanding which process is employed in fabricating the SGOI substrate, the relaxed SiGe layer 18 typically has a thickness from about 20 to about 80 nm, with a thickness from about 30 to about 50 nm being more typical. The term "relaxed SiGe layer" denotes a SiGe layer that has a measured degree of relaxation of about 35 % or greater, preferably 50 or greater. The term "SiGe" denotes a SiGe alloy having a Ge content between 0 to 100 atomic

percent, with a Ge content from about 10 to about 50 atomic percent being more typical.

[0035] The insulating layer 16 of the SGOI substrate may comprise an oxide, nitride, oxynitride or any combination thereof, with an oxide being most typical. The insulating layer 16 typically has a thickness from about 50 to about 300 nm, with a thickness from about 100 to about 150 nm being more typical. The thickness of the Si-containing substrate layer 14 is not critical to the present application and can vary over a wide range of thicknesses.

[0036] Stained Si layer 20 is formed atop the SGOI substrate 12, particularly on the relaxed SiGe layer 18, by an epitaxial deposition process well-known to those skilled in the art. The thickness of the strained Si layer 20 may vary, but typically, the strained Si layer 20 has a thickness from about 1 to about 100 nm. Because the relaxed SiGe layer 18 of the SGOI substrate 12 has a large in-plane lattice parameter as compared to the epi Si layer 20 formed thereon, the epi Si layer 20 will be strained in a tensile manner.

[0037] The gate dielectric 22, which is located atop the strained Si layer 20, comprises an oxide such as, for example, SiO_2, TiO_2, HfO_2, ZrO_2, Al_3O_4, mixed oxides such as per-

ovskite-type oxides and the like. In a preferred embodiment, gate dielectric 22 comprises SiO_2, or a nitrogen rich thermal oxide. The gate dielectric 22 can be formed by a deposition process such as, for example, chemical vapor deposition (CVD), plasma-enhanced chemical vapor deposition (PECVD), evaporation, chemical solution deposition, or atomic layer deposition (ALD). Alternatively, the gate dielectric 22 can be formed by a thermal oxidation process as well as a thermal oxidation under a nitrogen-containing environment. In a preferred embodiment in which SiO_2 is employed as the gate dielectric 22, thermal oxidation is used in forming the gate oxide. In some instances, typical nitrogen enriched technology such as plasma nitridation can be used in conjunction with thermal oxidation. When a thermal oxidation process is employed, the surface of the strained Si is typically cleaned with a conventional cleaning agent prior to thermal deposition of the oxide.

[0038] The thickness of the gate dielectric 22 formed atop the strained Si layer 20 may vary depending on the process used in forming the same as well as the type of insulator employed. Typically, however, the gate dielectric 22 has a thickness from about 0.5 to about 10 nm, with a thickness

from about 1 to about 3 nm being even more typical.

[0039] It is noted that prior to formation of the gate dielectric 22, various implants such as a well implant and a channel implant (both not shown) can be performed. The well implant, which typically forms a well region (not shown) within the relaxed SiGe layer 18, is carried out using a conventional ion implantation process well known to those skilled in the art. P- or N-type dopants can be used in forming the well region. Likewise, the channel implant, which forms a channel region (not shown) within the strained Si layer 20, is performed using a conventional ion implantation process that is also well known to those skilled in the art. The channel implant can be performed using N- or P-type dopants.

[0040] It is emphasized that the above processing occurs on an unpatterned structure that does not contain any trench isolation regions. Since the above process is performed first prior to trench isolation formation, there is no restriction on the amount of oxide removal which typically occurs in the prior art when the trench isolations are formed prior to gate dielectric formation. The multiple gate oxide process requires different amounts of oxide removal depending on the device location in prior art, in-

cluding STI (shallow trench isolation) height variation. However, this invention is free from the STI variation because the trench isolation region is not formed yet. Since there is no pattern used at this point of the present invention, an alignment key formation process may be required in some instances. The alignment key formation process includes depositing a CVD oxide on the strained Si surface, followed by lithography and a wet oxide etch process.

[0041] In accordance with the present invention, the structure at this point of the present invention will have a multiple gate thickness on the strained Si layer 20 with a variety of channel implantation on different areas within the structure.

[0042] Next, and as shown in FIG. 1B, a gate polySi (i.e., first polySi layer) 24 and a pad nitride layer 26 are formed on the initial structure 10 shown in FIG. 1A. Specifically, a layer of gate polySi 24 is formed on the surface of the gate dielectric 22 by a conventional deposition process including, for example, CVD, PECVD, evaporation, chemical solution deposition, ALD, and other like deposition processes. The gate polySi 24 formed at this point of the present invention has a thickness from about 50 to about

300 nm, with a thickness from about 100 to about 150 nm being more typical.

[0043] Pad nitride layer 26 is formed atop the gate polySi 24 by a deposition process such as CVD, PECVD, evaporation, chemical solution deposition and the like. The pad nitride layer 26 formed at this point of the present invention has a thickness from about 10 to about 100 nm, with a thickness from about 20 to about 50 nm being more typical.

[0044] It is noted that in the inventive process no pad oxide layer is employed. Instead, the pad oxide layer is replaced in the present invention by the combination of the gate dielectric 22 and the gate polySi 24. Various kinds of ions can be implanted into the gate polySi 24 depending on the circuit requirement before the pad nitride 26 deposition. It is also worth while pointing out the gate polySi 24 formed at this step of the present invention is confined to the active device area of the structure. A gate polySi layer can be formed atop the trench isolation (to be subsequently formed) during formation of self-aligned silicide contacts.

[0045] The structure shown in FIG. 1B is then patterned by lithography and etching so as to provide the patterned structure shown in FIG. 1C. Specifically, the lithography

and etching patterns the pad nitride layer 26, the gate polySi layer 24, the gate dielectric 22 as well as the stained Si layer 20 and the relaxed SiGe layer 18 into a first stack. The etching step employed in the present invention can have a lateral undercut or recess region 21 in the relaxed SiGe layer 18 beneath the strained Si layer 20.

[0046] The lithography step employed at this point of the present invention comprises applying a photoresist (not shown) to the surface of the pad nitride layer 26, exposing the photoresist to a pattern of radiation, and developing the pattern into the photoresist using a conventional resist developer. The lithographic step forms a patterned photoresist atop a predetermined portion of the pad nitride layer 26. The exposed regions, not including the patterned photoresist, are then etched using at least one etching step, stopping atop the insulating layer 16. The at least one etching step includes a dry etch process such as reactive-ion etching (RIE), ion beam etching, plasma etching, or laser ablation, a wet etching process, or any combination thereof. In a preferred etching scheme, the pad nitride layer 26 is first etched and then the patterned photoresist is stripped using a conventional stripping process. The patterned nitride layer 26 is then used as a mask for

etching the underlying layers forming the first stack atop the insulating layer 16.

[0047] The total thickness of the pad nitride layer 26 and the gate polySi 24 employed is typically similar or thicker than a conventional pad nitride layer. In the present invention, the total thickness of the pad nitride layer 26 and the gate polySi 24 is preferred to be thicker than a conventional pad nitride layer so as to be able to protect the sidewalls of the strained Si layer 20 during subsequent wet/dry etch processing to complete the final structure. Considering photoresist thickness restriction with a small ground rule, an oxide hard mask (not shown) can be used in the present invention, allowing a much thinner resist thickness than a conventional resist process. When an oxide hard mask is employed, it is typically formed atop the pad nitride layer 26 prior to lithography. Note that the pad nitride thickness is typically decided in the prior art by the height of the trench isolation regions. However, in the present invention, the trench isolation height is related to the sum of the pad nitride and polySi gate, allowing the use of a much thinner pad nitride layer than a conventional process.

[0048] Next, a trench oxide 28 such as tetraethylorthosilicate

(TEOS) or a high density plasma oxide is formed atop the exposed surface of the insulating layer 16, and the trench oxide 28 is then planarized by chemical mechanical polishing or grinding to provide the structure shown, for example, in FIG. 1D. A single or multiple deposition can be employed in the present invention in forming trench oxide 28. Trench oxide 28 forms the raised trench isolation regions of the inventive structure in regions adjacent to the first stack provided above. Note that the pad nitride layer 26 undergoes a deglazing step after planarizing the trench oxide 28, which causes the pad nitride layer 26 to extend above the upper planarized surface of the trench oxide 28. As shown in FIG. 1D, the recess area 21 is not filled with any material; instead, a void 25 remains in the structure. In some embodiments, an insulating material (not shown) can be used to fill the recess area 21 prior to forming the trench oxide 28.

[0049] The pad nitride layer 26 is now removed from the structure using a conventional stripping process that selectively removes nitride as compared to oxide or polySi. After removing the pad nitride layer 26, a polySi layer 30 is formed over the structure using a conventional deposition process. The polySi layer 30 formed at this point of the

present invention typically has a thickness after deposition from about 50 to about 200 nm, with a thickness from about 50 to about 100 nm being more typical.

[0050] Next, an insulator, such as a high temperature oxide (HTO), 32 is deposited with LPCVD atop the polySi layer 30. The insulator 32 has a thickness that is typically from about 10 to about 100 nm, with a thickness from about 10 to about 50 nm being more typical. Cap nitride 34 is then formed atop the insulator 32 by a conventional deposition process. The cap nitride 34 typically has a thickness from about 20 to about 80 nm, with a thickness from about 30 to about 50 nm being more typical. The resultant structure after pad nitride removal and formation of layers 30, 32, and 34, i.e., material layer 35, is shown in FIG. 1E. Note that in some regions polySi layer 30 is in contact with gate polySi 24.

[0051] Since the gate dielectric 22 has been formed prior to trench oxide 28 formation, no oxide is removed from the trench oxide 28, as typically is the case in prior art processes in which the trench oxide is formed prior to gate dielectric formation. Because of the inventive processing sequence, there is no variation in trench oxide height as is the case in the prior art process. Particularly, the inventive

processing sequence does not induce trench isolation height variation to the structure.

[0052] FIG. 1F shows the structure after the nitride cap 34, insulator 32, polySi layer 30 gate and polySi 24 have been patterned via lithography and etching into a second stack. Note that the second stack includes patterned elements from the first stack and it lies atop the gate dielectric 22. The gate dielectric 22 is not etched at this point of the present invention. The lithography and etching steps include the processing described above. Note that no extra gate poly over etching is required in the present invention once the gate polysilicon has been exposed. In the case of the conventional process flow, extra over etching is required (as much as the trench isolation height) since the gate polySi thickness at the interface is thicker than the deposited thickness. In the present invention, however, the maximum gate polySi thickness is the same as the gate polySi thickness of the active region. Once the gate poly on the active area is removed, all other regions are already cleared of polySi. A significant advantage can be obtained when ultra thin (on the order of about 1 nm or less) gate oxides are employed.

[0053] Next, and as shown in FIG. 1G, a sacrificial nitride spacer

36 is formed on exposed sidewalls of the structure shown in FIG. 1F. In particular, a sacrificial nitride spacer 36 is formed on exposed sidewalls of layers 34, 32, 30, 24, 22 and trench oxide 28. The sacrificial nitride spacer 36 is formed by deposition and dry etching.

[0054] At this point of the present invention, any gate dielectric 22 not protected by the second stack or the sacrificial nitride spacers 36 is removed to expose underlying surfaces of the strained Si layer 20. A wet etch process can be used to remove the unprotected portions of the gate dielectric 22.

[0055] A selective epitaxial Si layer 38, which becomes the elevated source/drain region of the inventive structure, is then formed via a conventional epi growth process atop the exposed surfaces of the strained Si layer 20, see FIG. 1H. Note that the selective epitaxial Si layer 38 growth requires a strong pre-clean which can potentially remove a significant amount of oxide. In the present invention, the sacrificial nitride spacers 36 protect oxide from being removed. Specifically, the spacer 36 prevents the void 25 from being exposed during precleaning. The void 25, which is formed naturally in this embodiment, is not preferred, but, with spacer 36 in accordance with this inven-

tion, can be tolerated.

[0056] The sacrificial nitride spacers 36 are then removed from the structure utilizing a wet etch process that selectively removes nitride. Note that small voids (or divots) labeled as 40 in FIG. 1I are formed. At this point of the inventive process, any implantation can be performed for device control (e.g., threshold voltage control). Note during the removal of the sacrificial nitride spacers 36, the nitride cap 34 is also removed exposing oxide 32.

[0057] The divots 40 shown in FIG. 1I are then filled with a nitride fill material 42 providing the structure shown in FIG. 1J. The nitride fill material 42 is formed into the divots 40 by depositing a layer of nitride, and wet etching the deposited nitride layer.

[0058] Next, oxide spacers 44 are formed on exposed sidewalls of the oxide 30, and gate polySi 24 by deposition and etching providing the structure shown, for example, in FIG. 1K. Specifically, the structure shown in FIG. 1J includes an active device region 100 comprising relaxed SiGe layer 18, strained Si layer 20 located atop the relaxed SiGe layer 18, a raised source/drain region 38 located atop a portion of said strained Si layer 20, and a second stack comprising at least gate dielectric 22 and gate

polySi 24, 30 located on another portion of the strained Si layer 20; and a raised trench oxide region 28 surrounding the active device region 100.

[0059] Depending on the transistor performance requirement, multiple disposable spacers can be formed without hurting the philosophy of the invention.

[0060] After forming the oxide spacers 44 typical CMOS processing such as silicide contact formation can be performed.

[0061] While the present invention has been particularly shown and described with respect to preferred embodiments, it will be understood by those skilled in the art that the foregoing and other changes in forms and details may be made without departing from the spirit and scope of the present invention. It is therefore intended that the present invention not be limited to the exact forms and details described and illustrated, but fall within the scope of the appended claims.

[0062] What is claimed is: